POSITAL
FRABA

BiSS C to SSI / SPI adaption – short form

<u>Applicable for:</u>

Multiturn Kit: **KCD-BC00B-1617-U01x-JAQ**

Evaluation Kit: **KCD-BC00B-1617-BRRx-2RW**

Copyright ©FRABA

Date 20171218

POSITAL
FRABA

BiSS C to SSI / SPI adaption for a Multiturn Encoder

Hardware Adaption

- Not necessary
- RS-422, RS-485 needed
- Design can be kept like for SSI

Software Adaption

- Minor bit stream analysis
- Because of overhead in BiSS protocol compared to SSI more bits are needed to be read out.
- Data stream must be analyzed to find a short signature to locate the start position of position value within the bit stream
- Easy implementation via SPI for many MCU

Copyright ©FRABA

POSITAL
FRABA

Differences of SSI to BiSS C Protocol for a Multiturn Encoder

Definition of SSI

In SSI protocol the data stream just contains the position value with Multiturn and Singleturn bits.

Definition of BiSS C

In BiSS C protocol more bits shall be read out as seen above for SSI, because of busy time, signature, diagnostics and CRC sequence. Because of these additional information some adaptions are needed in the PLC to mask out some bits to get just the position value. The busy time is set to constant 7µs and shall be read out by dummy bits, which number is depending on configured clock frequency from PLC.

Copyright ©FRABA

POSITAL
FRABA

Recommended Implementation of BiSS C via SPI

- Define the clock frequency used in your PLC, recommended max. 2MHz to prevent considerations of latency times.
- Decide, if you want to read in diagnostic bits (error + warning bit) and CRC field or abort earlier the transmission.
- Calculate number of needed clock cycles for busy time, Busy Time = 7µs / T_clock frequency.
- Generate in PLC the clock burst sequence and read in data signal on falling edge of clock pulse
- After reading in of complete sequence search in the serial data stream for the leading two bits with “1” as protocol check and the tailoring signature bits (last “0” from busy time and “1”,”0”) to find the location of the position value. With consideration of last “0” from busy bit a differentiation of the start phase is possible.
- Mask out by logical AND operation the not needed bits and shift the value for further arithmetic calculation right aligned. Shifting should be done as logical shift to prevent carry flag.

Copyright ©FRABA

POSITAL
FRABA

APPENDIX: Detailed Data Stream Explanation

Latch:	First rising edge of clock signal latches encoder position
Busy Time:	Indicated as ACK, With second rising edge of clock signal the encoder sends “0” until data processed internal and ready to send. This takes approximately 5.5 µs. <u>This time is not constant and might vary.</u> It is recommended to add one 1µs for safety reasons. Depending of the used clock frequency (CLK) the number of cycles must be adapted. Example: CLK frequency of 2.6 MHz. Busy time ~ 5.5µs + 1 µs ~ 6.5µs. Number of needed CLK pulses: 14 to 16 CKL pulses.
Signature	consists of 2 bits: Start: Encoder is ready to transmit data indicated by “1” CDS: Is always “0” in unidirectional mode, that means for SSI operation
Position Value	Consists of Multiurn (MT) 16 bit Singletrun (ST) 17 bit
Diagnostics	Error: e.g. HW-failure detected like memory. 0 = failure, 1 = data valid Warning: currently not supported. Constant =“1”. 0 = failure, 1 = good
CRC	Checksum. Inverted. See app note. http://www.biss-interface.com/files/BiSS_AN3_appnote_E1en.pdf
Time Out	Corresponds to tm at SSI, tm=12µs. It is shorter than standard SSI tm = 20 µs, but allows to have interface cycle of 50µs starting with 1MHz CLK

Copyright ©FRABA